ABSTRACT OF THE DISCLOSURE

A methodology for improving the timing of specific critical paths in a Field Programmable Gate Array (FPGA) implementation of a logic circuit without significantly affecting the timing of other logic paths. The method utilizes logic replication and specific guidelines for placement of the logic gates involved in a critical path to optimize the timing of that critical path. The logic gates involved in a critical path are either replicated and placed, or simply moved, in order to implement the desired logic with nearly the shortest total distance for routing of signals involved in the critical path. The optimization is carried out with relatively little impact on the timing of other paths and is applicable to FPGAs in which the signal delay between any source and gate is relatively independent of the fanout of the source signal to any other loads.